



S. S. EDUCATION TRUST'S
S.G. BALEKUNDRI INSTITUTE OF TECHNOLOGY, BELAGAVI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGBIT/ACA/02-R2
CLASS: VII (A) SEMESTER
ACADEMIC YEAR: 2022-23

TIME-TABLE

ROOM. NO.: B-120
W.E.F: 19-09-2022

DAY/TIME	9:15-10.15 am	10.15-11.15 am	11.15-11.30 am	11.30-12.30 pm	12.30-1.30 pm	1:30-2:30 pm	2.30-3.20 pm	3.20-4.10 pm	4.10-5.00 pm	BATCH	USN
MONDAY	CN	RTS	BREAK	VLSI	PROJECT	LUNCH BREAK	CNL-A2/VLSIL-A1		A ₁	2BU18EC027 TO 2BU19EC024	
TUESDAY	VLSI	OE		AE/MMC	VLSIL(T)		PLACE MENT	A ₂			2BU19EC025 TO 2BU19EC404
WEDNESDAY	RTS	OE		VLSIL(T)	CN						
THURSDAY	AE/MMC	OE		CN	CNL(T)						
FRIDAY	RTS	CNL(T)		VLSI	AE/MMC						
SATURDAY	CNL-A1/VLSIL-A2				PROJECT						

SUBJECT CODE	SUBJECT NAME	SUBJECT INITIALS	FACULTY NAME	HOURS/WEEK (L+T+P)	HOURS/WEEK AS PER VTU SCHEME (L+T+P)	TECH. STAFF NAME (For Labs)
18EC71	COMPUTER NETWORKS	CN	MR. ANANDREDDI N.	3+0+0	3+0+0	
18EC72	VLSI DESIGN	VLSI	MRS. SOUMYA HALAGATTI	3+0+0	3+0+0	
18EC731	REAL-TIME SYSTEMS	PE2	MS. MEGHA KARABASHETTI	3+0+0	3+0+0	
18EC742/ 18EC743	AUTOMOTIVE ELECTRONICS/ MULTIMEDIA COMMUNICATION	PE3	MR. SUJAY GEJJI/ MR. ANANDREDDI N.	3+0+0	3+0+0	
18EC742	OE-B	OE		3+0+0	3+0+0	
18ECL76	COMPUTER NETWORK LAB	CNL	MR. ANANDREDDI N.	0+2+2	0+2+2	
18ECL77	VLSI LAB	VLSIL	MRS. SOUMYA HALAGATTI	0+2+2	0+2+2	MR. VIJAY M
18ECP78	PROJECT WORK PHASE 1	PWP	MR. SHANKARGOUDA	0+0+2	0+0+2	
-	INTERNSHIP	INT	MRS. SHILPA B	-	-	

CLASS TEACHER- MR. ANANDREDDI N.

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 DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SGBIT/ACA/02-R2
 CLASS: VII (B) SEMESTER
 ACADEMIC YEAR: 2022-23

TIME-TABLE

ROOM. NO.: B-121
 W.E.F: 29-09-2022

DAY/TIME	9:15-10.15 am	10.15-11.15 am	11.15-11.30 am	11.30-12.30 pm	12.30-1.30 pm	1:30-2:30 pm	2.30-3.20 pm	3.20-4.10 pm	4.10-5.00 pm	BATCH	USN	
MONDAY	VLSI	CN	BREAK	RTS	VLSIL(T)	LUNCH BREAK				B ₁	2BU19EC004 TO 2BU19EC068	
TUESDAY	CN	OE		AE/MMC	PROJECT		PLACE MENT					
WEDNESDAY	VLSIL(T)	OE		CN	RTS		CNL-B1/VLSIL-B2				B ₂	2BU18EC069 TO 2BU19EC406
THURSDAY	AE/MMC	OE		VLSI	CNL(T)		CNL-B2/VLSIL-B1					
FRIDAY	RTS	VLSI		CNL(T)	AE/MMC							
SATURDAY	PROJECT											

SUBJECT CODE	SUBJECT NAME	SUBJECT INITIALS	FACULTY NAME	HOURS/WEEK (L+T+P)	HOURS/WEEK AS PER VTU SCHEME (L+T+P)	TECH. STAFF NAME (FOR LABS)
18EC71	COMPUTER NETWORKS	CN	MR. GIRISH K	3+0+0	3+0+0	
18EC72	VLSI DESIGN	VLSI	MRS. SOUMYA H	3+0+0	3+0+0	
18EC731	REAL TIME SYSTEMS	RTS	MR. SIDRAMAYYA MATAD	3+0+0	3+0+0	
18EC742/ 18EC743	AUTOMOTIVE ELECTRONICS/ MULTIMEDIA COMMUNICATION	AE/ MMC	MR. SUJAY GEJJI/ MR. ANANDREDDI N.	3+0+0	3+0+0	
18EC742	OE-B	OE		3+0+0	3+0+0	
18ECL76	COMPUTER NETWORK LAB	CNL	MR. GIRISH K	0+2+2	0+2+2	
18ECL77	VLSI LAB	VLSIL	MR. NARAYAN A.B.	0+2+2	0+2+2	MR.VUAY
18ECP78	PROJECT WORK PHASE 1	PWP	MR. SHANKARGOUDA	0+0+2	0+0+2	
-	INTERNSHIP	INT	MRS. SHILPA B			

CLASS TEACHER- MR. SIDRAMAYYA M

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9/8/22
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28/9/22
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 DR. ASHOK M. HULAGABALI
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8/9/22
 DR. B. R. PATAGUNDI
 PRINCIPAL
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